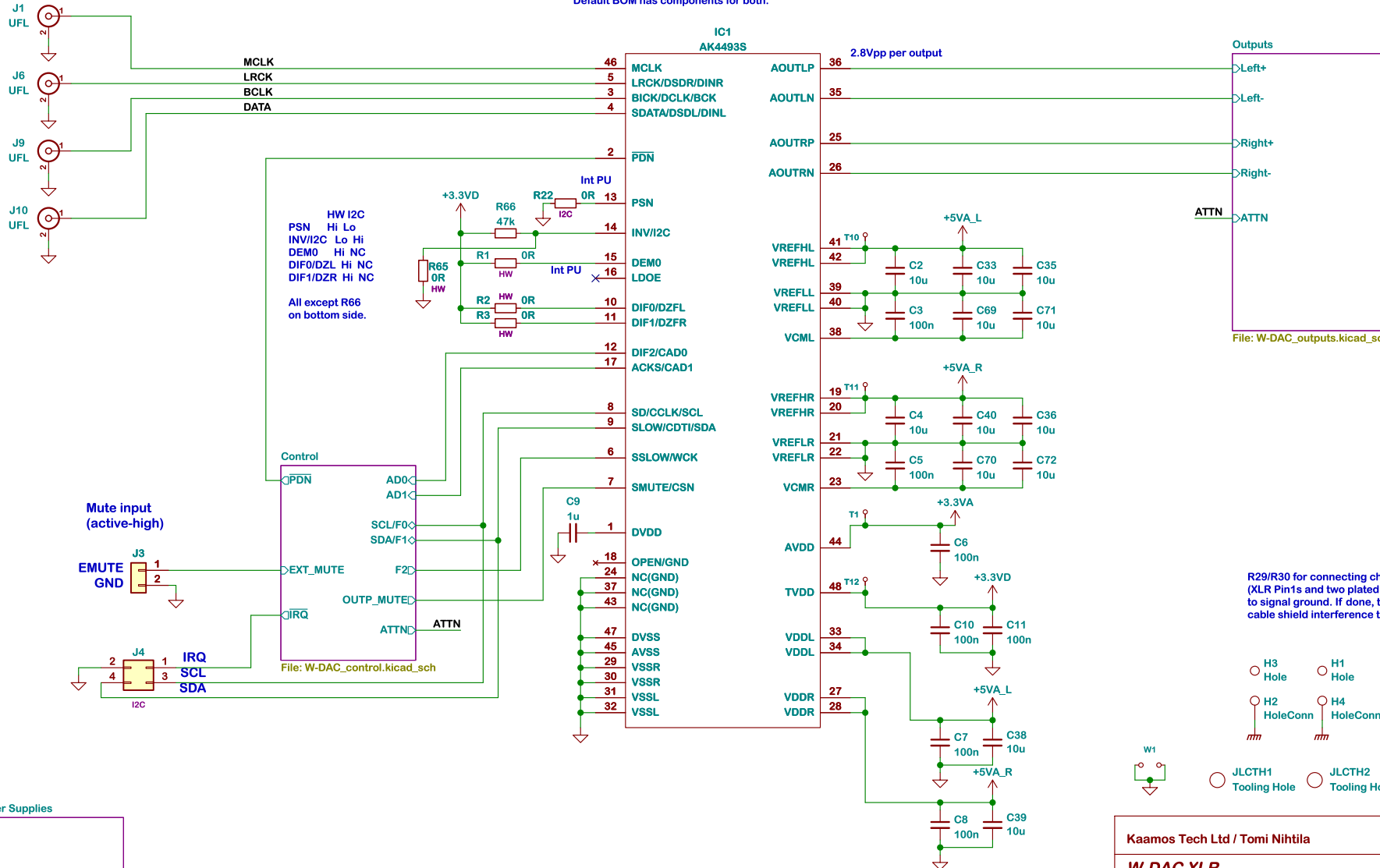


W-DAC XLR v1.1

Root sheet

Two variants: A) HW-control B) I2C-control.
Default BOM has components for both.

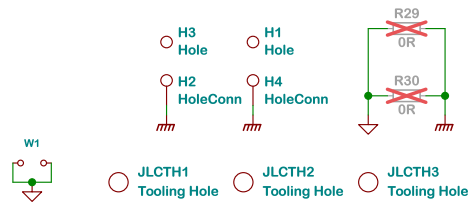


File: W-DAC_outputs.kicad_sch

File: W-DAC_control.kicad_sch

Power Supplies
File: W-DAC_PSU.kicad_sch

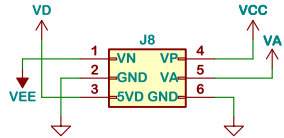
R29/R30 for connecting chassis ground (XLR Pin1s and two plated mounting holes) to signal ground. If done, this may direct cable shield interference to audio ground.



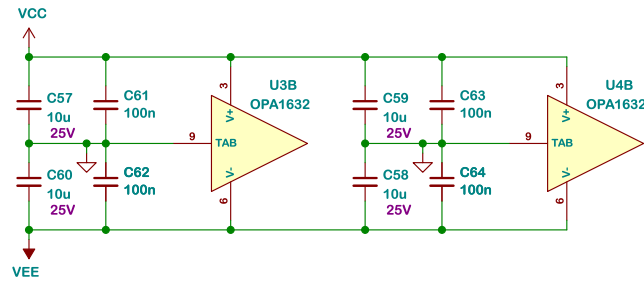
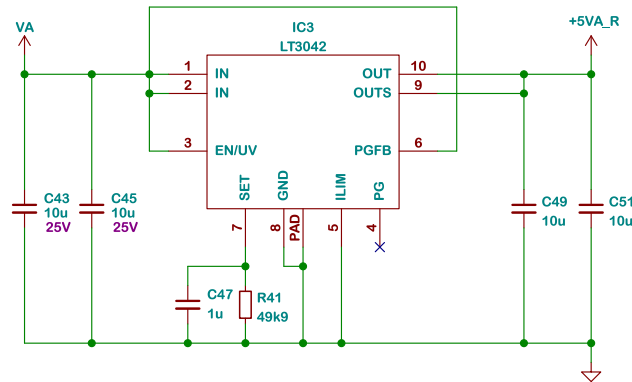
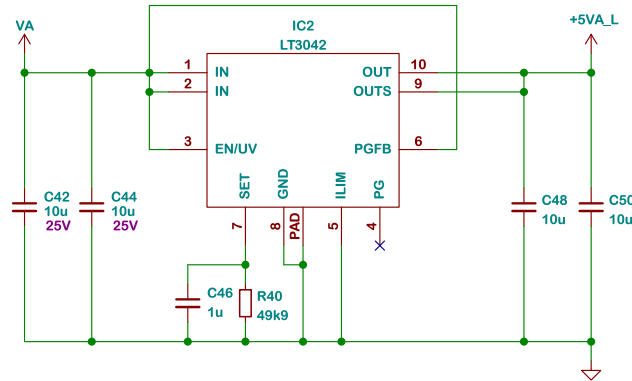
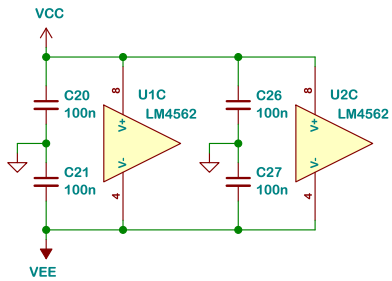
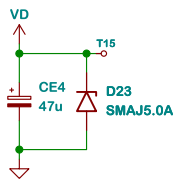
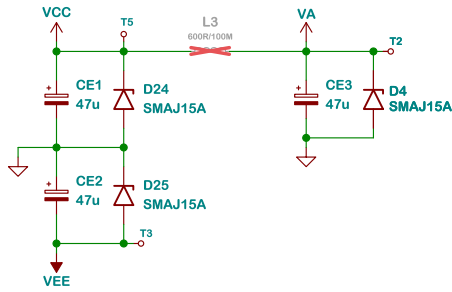
Kaamos Tech Ltd / Tomi Nihtila		
W-DAC XLR		
Sheet: /		
File: W-DAC.kicad_sch		
Size: A4	Date: 2024-06-18	Rev: v1.1
KiCad E.D.A. 8.0.6		Id: 1/4

Power Supplies

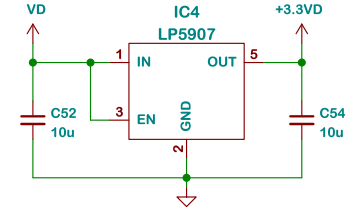
Analog supplies



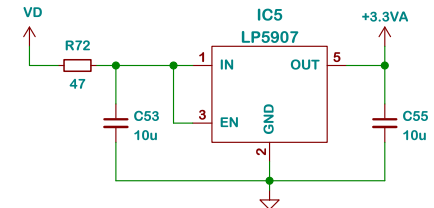
If separate VA is not used, VCC can be used by populating L3 (bottom side). Make sure VA is not connected to any other board or PSU via J8 that may get damaged by high VA!



DVDD Supply



AVDD Supply (clock interface supply)



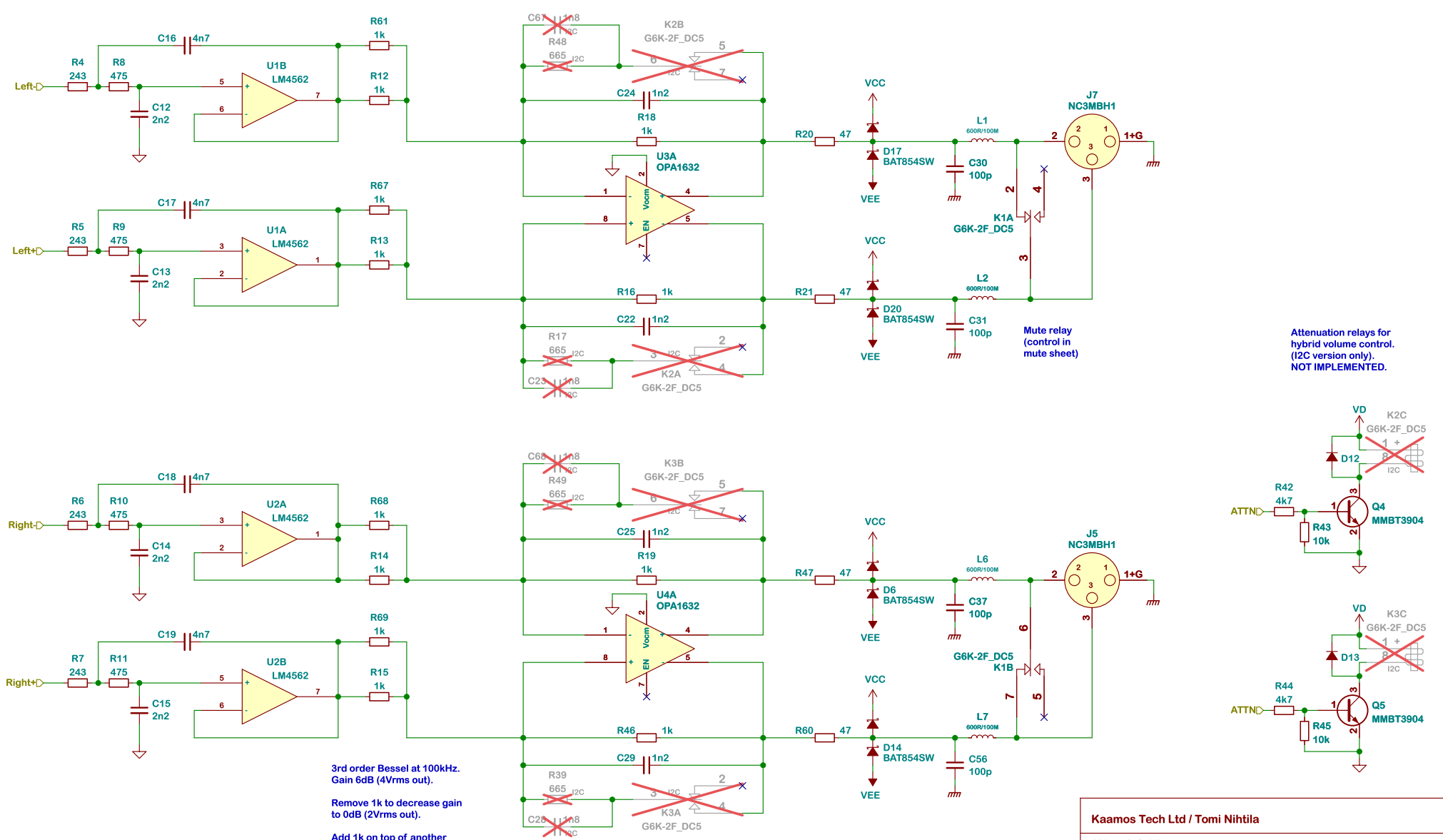
Kaamos Tech Ltd / Tomi Nihtila

W-DAC XLR

Sheet: /Power Supplies/
File: W-DAC_PSU.kicad_sch

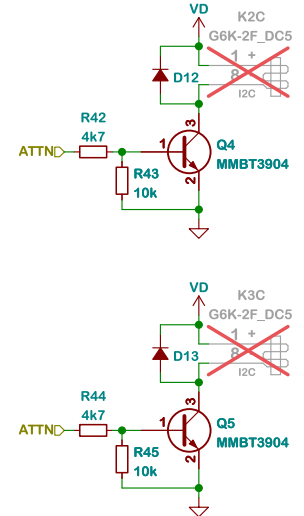
Size: A4	Date: 2024-06-18	Rev: v1.1
KiCad E.D.A. 8.0.6		Id: 2/4

Outputs



Attenuation relays for hybrid volume control. (I2C version only). NOT IMPLEMENTED.

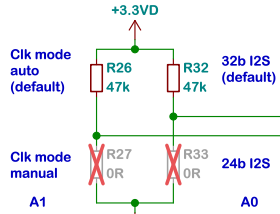
3rd order Bessel at 100kHz. Gain 6dB (4Vrms out).
 Remove 1k to decrease gain to 0dB (2Vrms out).
 Add 1k on top of another (500R in parallel with 1k) for 9.5dB gain (6Vrms out).



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W-DAC XLR		
Sheet: /Outputs/ File: W-DAC_outputs.kicad_sch		
Size: A4	Date: 2024-06-18	Rev: v1.1
KiCad E.D.A. 8.0.6		Id: 3/4

Control

Clocking and data in HW-mode, address pins in I2C-mode.



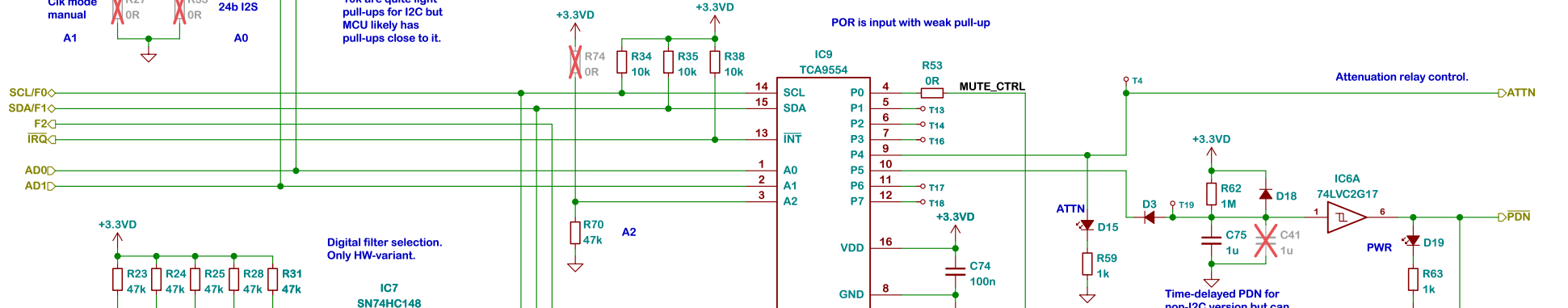
I2C/Fx pins are SCL/SDA in I2C-mode and filter selection in HW-mode.

10k are quite light pull-ups for I2C but MCU likely has pull-ups close to it.

I2C addresses:
AK4493S: 0010 0 A1 A0 RW (def 7-bit 0x13)
TCA9554: 0100 A2 A1 A0 RW (def 7-bit 0x23)

A-resistors are on bottom side.

POR is input with weak pull-up



Digital filter selection. Only HW-variant.

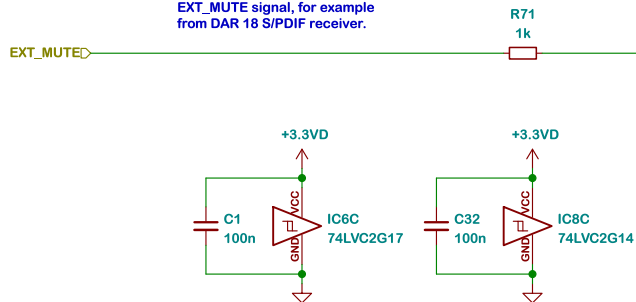


SSLOW SLOW SD

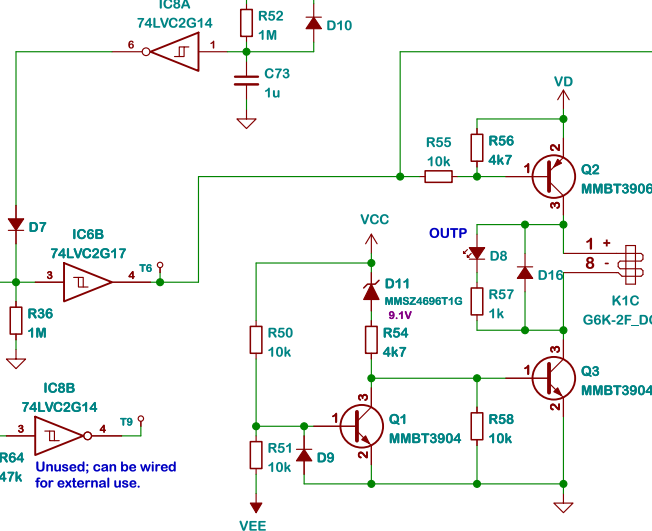
Filter setting:	A2	A1	A0
Sharp	0	0	0
Slow	0	1	0
SD Sharp	0	0	1
SD Slow	0	1	1
S-Slow	1	x	0
LD Short	1	x	1

x = Don't care

EXT_MUTE signal, for example from DAR 18 S/PDIF receiver.



Prevents unmute if DAC power is down. Delay for unmute when DAC powers up.



Time-delayed PDN for non-I2C version but can be overridden by control signal from TCA9554.

Mutes DAC IC as well.

Mute and supply monitor.

- Mute releases in following conditions:
- OUTP_MUTE is low.
- 5VD supply is up.
- VCC and VEE are up.
- VCC and VEE are (fairly) symmetrical.

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W-DAC XLR

Sheet: /Control/

File: W-DAC_control.kicad_sch

Size: A4

Date: 2024-06-18

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Id: 5/4